Agenda for today

Hochschule RheinMain

- Discussion of chapter on caches (03b-caches)

Feedback: some questions (1)

Hochschule RheinMain

- Explain, how caches make use of *temporal and spatial locality* to improve average performance.
- What about worst case performance? How (if at all) is it affected by the use of caches?
- How is a cache organised, i.e.
  - What is its smallest unit of data ?
  - Which items of state are kept per unit? What is their function?

Feedback: some questions (2)

Hochschule RheinMain

- Explain virtually indexed vs. physically indexed caches.
- In a cache architecture having 4096 sets, how many address bits would be used for the index?
- What are the higer address bits used for?
- Explain direct mapped, n-way set associative and fully associative caches and the tradeoff between them.
- Why not make all caches fully associative?

Feedback: some questions (3)

Hochschule RheinMain

- Explain the four types of possible cache misses (the *four Cs*):
  - Compulsory miss
  - Capacity miss
  - Conflict miss
  - Coherence miss
- Explain some cache replement policies, i.e. LRU, Random, Toss Clean
- Explain some cache write policies, i.e. write back/write through

Feedback: some questions (4)

Hochschule RheinMain

- In the context of caches and MMUs, what are
  - Homonyms?
  - Synonyms?
- Which types of Caches (VV, VP, PP) are potenially affected by these?
- How can Synonym problems be avoided?

Feedback: some questions (5)

Hochschule RheinMain

- Explain the motivation for having a write buffer.
- What is a “Harvard Architecture“ and why can having seperate I- and D-Caches be seen as such?
- What is the function of a *Translation Lookaside Buffer* (TLB)?